High-Level Simulation of Chua's Circuit to Verify Frequency Scaling Behavior

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Abstract. This work describes a high-level simulation technique to verify frequency-scaling behavior of Chua's circuit. Chua's diode is modeled by a piecewise-linear approximation which is simulated by using and combining Verilog and HSPICE. The frequency-scaling behavior is measured by both Verilog and HSPICE, and the last one is used to simulate the frequency spectrum to confirm the scaling.

1 Introduction

Nowadays, the electronic design automation (EDA) community is developing high-level simulation tools to help the designers to verify their design before the physical implementation. In this manner, hardware description languages (HDLs), such as Verilog [1], provides the environment to describe an electronic design at a level of abstraction higher than the transistor one, which is done normally in circuit design using HSPICE. Furthermore, it is possible to combine an HDL software (Verilog) with a transistor software (alike HSPICE) [2], in order to cover the gap between high-level to physical descriptions. That way, a designer can start the circuit description using equations within Verilog, and then gradually he can make a refinement process until obtaining a design at the transistor level using HSPICE. For instance, in [3] it is shown the high-level modeling of Chua's circuit using state variables and piecewise-linear (PWL) approximation [4], and in [5] is shown the implementation at the transistor level of abstraction.

Chaotic systems such as Chua's circuit can be described from high-level (Verilog) to circuit level (HSPICE). In this manner, the nonlinear element, i.e. Chua's diode, can be easily described by Verilog using PWL approximation in order to verify frequency-scaling behavior of the chaotic oscillator before its physical realization.

Chua's circuit is shown in Fig. 1(a). The PWL approximation of Chua's diode (N_R) is shown in section 2. Its Verilog description is derived in section 3. The HSPICE description is shown in section 4 along with the simulations using Verilog

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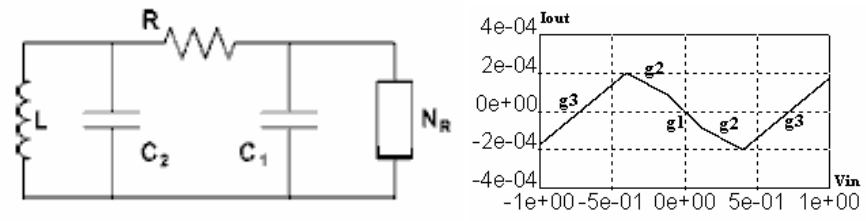
and HSPICE. The frequency-scaling behavior and the frequency spectrum simulations are shown in section 5. Finally, the conclusions are summarized in section 6.



(a) (b)

Fig. 1. (a) Chua's chaotic oscillator, and (b) I-V characteristic of Chua's diode

2 PWL Approximation of Chua's Diode

According to [3], a third order chaotic oscillator can be described using only passive components except for N_R, as shown in Fig. 1. The system described by (1) depends on an initial condition, e.g. a voltage across a capacitor (Vc_1 or Vc_2) or a current through the inductor (I_L) to perform an oscillating behavior. The nonlinear component (N_R) enhances this oscillation and produces instability according with the I-V characteristic shown in Fig. 1(b). Basically, it performs the behavior of a two negative voltage to current slope device; the positive slopes have no effect on the chaotic phenomena but are generally presented by the nonlinear circuit. By using the values derived in [3], the slopes and break point values are: $g_1 = 1/1358$, $g_2 = 1/2464$, $g_3 = 1/1600$, $B_1 = \pm 0.114$V and $B_2 = \pm 0.4$V. The behavior of Chua's diode is described by (2). By setting $C_1 = 450$pF, $C_2 = 1.5$nF, L = 1mH, R = 1650Ω, these values maintain chaotic oscillation and scroll generation [3]. However, C_1, C_2, and L will be modified herein to show frequency-scaling behavior.

$$\begin{bmatrix} \frac{d}{dt}Vc_1 \\ \frac{d}{dt}Vc_2 \\ \frac{d}{dt}i_L \end{bmatrix} = \begin{bmatrix} -1/RC_1 & 1/RC_1 & 0 \\ 1/RC_2 & -1/RC_2 & 1/C_2 \\ 0 & -1/L & 0 \end{bmatrix} \begin{bmatrix} Vc_1 \\ Vc_2 \\ i_L \end{bmatrix} + \begin{bmatrix} i_{NR}/C_1 \\ 0 \\ 0 \end{bmatrix} \tag{1}$$

$$i_{NR} = \begin{cases} g_2 Vc_1 + (g_2 - g_1)B_1 & ....Vc_1 < -B_1 \\ g_1 Vc_1 & -B_1 < Vc_1 < B_1 \\ g_2 Vc_1 + (g_1 - g_2)B_1 & Vc_1 > B_1 \end{cases} \tag{2}$$

3 PWL Verilog-A Description

Chua's diode can be described by an I/V PWL function consisting of three different segments S_i parameterized by slopes g_i and breakpoints B_j which complete equations are given in (3) for a semi-plane X (positive/negative).

The I/V behavior is described by the Verilog sentence given in (4), as it is done in [2]. $f(V)$ is the PWL function from Fig. 2, and its Verilog description is:

```
module fchua(x,y,g);
        input x;
        output y;
        electrical y,x,g;
        real res;
        analog begin
                if (V(x,g) < -0.4)
                res = V(x,g)/1600+4.500184e-4;
                else if ((V(x,g) > -0.4)&&(V(x,g) < -0.114))
                res = -V(x,g)/2464+3.76807e-5;
                else if ((V(x,g) > -0.114)&&(V(x,g)< 0.114))
                res = -V(x,g)/1358;
                else if ((V(x,g) > 0.114)&&(V(x,g) < 0.4))
                res = -V(x,g)/2464-3.76807e-5;
                else
                res = V(x,g)/1600-4.500184e-4;
                I(g,y) <+ -res;
        end
endmodule
```

$$
\begin{aligned}
S_1(x) &= -\frac{1}{1358}x \\
S_2(x) &= -\frac{1}{2464}x \;\mu\; 37.6807 * 10^{-6} \\
S_3(x) &= \frac{1}{1600}x \;\mu\; 450.0184 * 10^{-6}
\end{aligned}
\tag{3}
$$

$$
I(out,gnd) <+ f(V(in,gnd)) \tag{4}
$$

4 Verilog-A and HSPICE Simulations

The HDL description, as the one shown in section 3, can be added to a more large circuit or system to prove its functionality using either or both Verilog and HSPICE. For instance, the comparison results between Verilog and HSPICE will confirm that this simple model has good approach with reality as concluded in [3],[5]. Furthermore, Chua's circuit was simulated by using Verilog-A to reproduce the chaotic phe-

nomena shown in [5], by adjusting R. The voltage responses across the capacitors are shown in Fig. 2.

The HSPICE description of the I/V PWL behaviour of Chua's diode is done using a PWL polynomial voltage controlled current source, as follows:

```
GCHUA  1        0        PWL(1)  1        0        DELTA=0.001
+-10,'-5.8e-3' -0.4,'0.00020002' -0.11,'8.3947E-5'
+0.11,'-8.3947E-5' 0.4,'-0.00020002' 10,'5.8e-3'
```

In Fig. 3 is shown the HSPICE simulation of Chua's circuit, so that one can conclude that the circuit keeps its behaviour when using either HSPICE or Verilog-A.

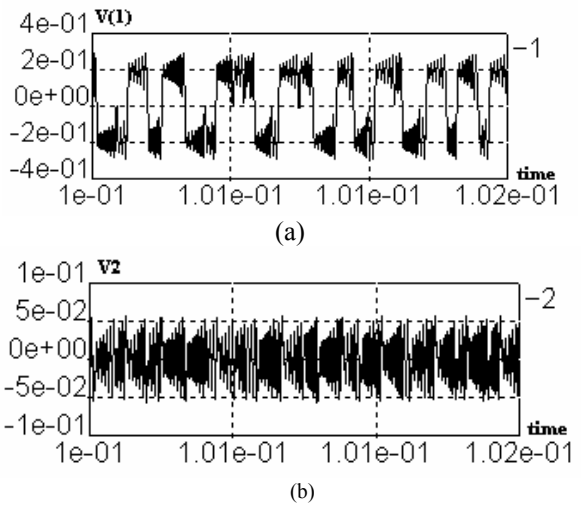


Fig. 2. Voltages across capacitors: (a) Vc_1 and (b) Vc_2

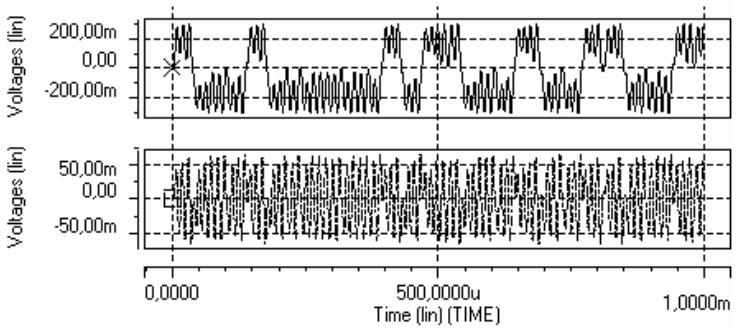


Fig. 3. Hspice response of the chaotic oscillator

The states trajectories (Vc_1 vs Vc_2) can be seen in Fig. 4.

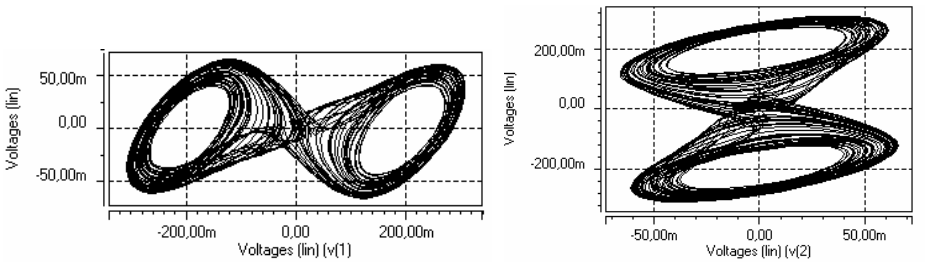


Fig. 4. State trajectories: Vc_1 vs Vc_2

5 Frequency Scaling Behavior

Chua's circuit can be used in secure communication systems as shown in [6]. Besides, it is quite convenient to verify its behavior at various ranges of frequency to cover wider applications. In [7] it is introduced an intelligent system to generate analog circuits which can be used to design Chua's diode and to reach higher frequencies. For instance, in this section is shown that by scaling the values of the capacitors and the inductor, Chua's circuit can scale its frequency spectrum.

From the results shown in Fig. 4(a), in Fig. 5 to Fig. 8 are shown chaotic oscillations which were scaled by 10, 1/2, 1/10 and 1/100, respectively. That is, each capacitor and the inductor are multiplied by the scaling factor. In each figure it is shown the behavior of the frequency spectrum, where x means mega Hertz on the horizontal axe.

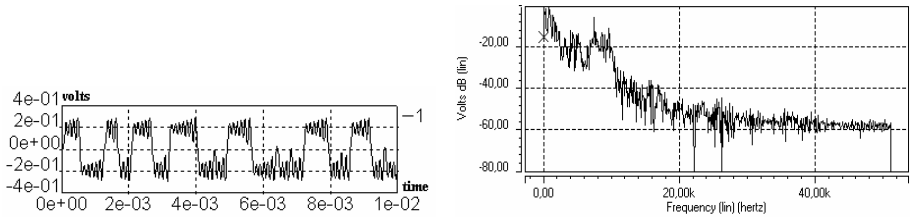


Fig. 5. Chaotic oscillation measured in Vc_1 at a scaling factor = 10, and its frequency spectrum

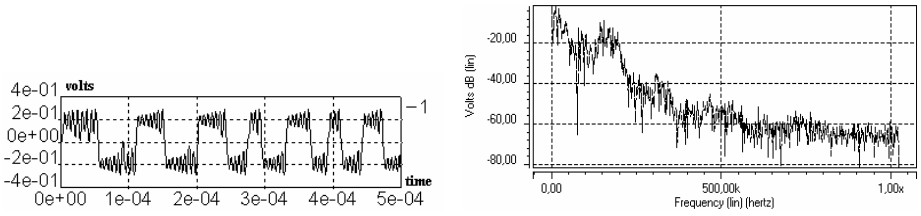


Fig. 6. Chaotic oscillation measured in Vc_1 at a scaling factor = 1/2, and its frequency spectrum

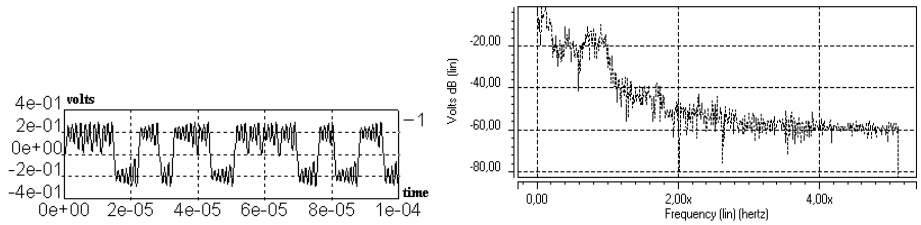


Fig. 7. Chaotic oscillation measured in Vc_1 at a scaling factor = 1/10, and its frequency spectrum

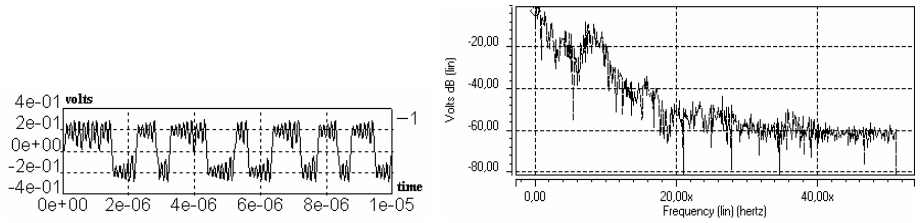


Fig. 8. Chaotic oscillation measured in Vc_1 at a scaling factor = 1/100, and its frequency spectrum

6 Conclusions

It has been shown the description of Chua's diode by using Verilog and HSPICE. Simulation results show that PWL approximation is suitable to verify the frequency scaling behaviour of Chua's circuit. Furthermore, it was shown that the frequency scaling presents a linear dependence with the component values. However, physical implementation will depend on the frequency limits of the analog circuits.

Equivalences between the Verilog-A models and Hspice models have been highlighted in order to prove sufficient concordance of both languages to describe circuits as macro-models giving hierarchy, simplicity and speed.

Acknowledgment

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